

AMENDMENT AND RESPONSE

Serial Number: 08/903,453

Filing Date: July 29, 1997

Title: CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS

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Please add the following new claims:

20.(New) A memory cell comprising:
a floating gate; and
a layer of amorphous carburized silicon between the floating gate and a substrate.

21.(New) The memory cell of claim 20, further comprising:
a source region in the substrate;
a drain region in the substrate;
a channel region in the substrate between the source region and the drain region, the channel region being separated from the floating gate by the layer of amorphous carburized silicon; and
a control gate separated from the floating gate.

22.(New) The memory cell of claim 20 wherein the substrate comprises a semiconductor surface layer on an underlying insulating portion.

23.(New) The memory cell of claim 20 wherein the substrate comprises a doped silicon semiconductor substrate.

24.(New) A transistor comprising:
a source region in a substrate;
a drain region in the substrate;
a channel region between the source region and the drain region in the substrate; and
a gate separated from the channel region by a layer of amorphous carburized silicon.

25.(New) The transistor of claim 24 wherein the gate comprises a floating gate.

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26.(New) The transistor of claim 25, further comprising a control gate separated from the floating gate.

27.(New) The transistor of claim 24 wherein the substrate comprises a semiconductor surface layer on an underlying insulating portion.

28.(New) The transistor of claim 24 wherein the substrate comprises a doped silicon semiconductor substrate.

29.(New) A semiconductor device comprising:
a first conductive layer supported by a substrate;
a layer of amorphous carburized silicon over the first conductive layer; and
a second conductive layer over the layer of amorphous carburized silicon.

30.(New) The semiconductor device of claim 29, further comprising a source/drain diffusion in the substrate below the first conductive layer.

31.(New) The semiconductor device of claim 29 wherein:
the first conductive layer comprises polysilicon; and
the second conductive layer comprises polysilicon.

32.(New) A memory cell comprising:
a first conductive layer supported by a substrate;
a layer of amorphous carburized silicon over the first conductive layer; and
a second conductive layer over the layer of amorphous carburized silicon.

33.(New) The memory cell of claim 32, further comprising a source/drain diffusion in the substrate below the first conductive layer.

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34.(New) The memory cell of claim 32, further comprising one or more word lines supported by the substrate.

35.(New) The memory cell of claim 32 wherein:
the first conductive layer comprises polysilicon; and
the second conductive layer comprises polysilicon.

36.(New) A capacitor comprising:
a first conductive layer supported by a substrate;
a layer of amorphous carburized silicon over the first conductive layer; and
a second conductive layer over the layer of amorphous carburized silicon.

37.(New) The capacitor of claim 36, further comprising a source/drain diffusion in the substrate below the first conductive layer.

38.(New) The memory cell of claim 36 wherein:
the first conductive layer comprises polysilicon; and
the second conductive layer comprises polysilicon.

REMARKS

In response to the Office Action mailed April 27, 1999, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 1-6 are pending in the application, and are rejected. Claims 3 and 4 have been amended, and new claims 20-38 have been added. No new matter has been added.

Rejection Under 35 U.S.C. 112

Claim 3 was rejected under 35 U.S.C. 112. The applicant respectfully traverses. Claim 3 has been amended to obviate the rejection.